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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,308	07/18/2005	Anthony Spencer	0120-033	1129

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EXAMINER	
THOMPSON, JR, OTIS L	
ART UNIT	PAPER NUMBER
2619	

NOTIFICATION DATE	DELIVERY MODE
05/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/534,308	SPENCER ET AL.	
	Examiner	Art Unit	
	OTIS L. THOMPSON, JR	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9,10 and 12-25* is/are rejected.

7)☒ Claim(s) *7,8 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/09/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 9, 10, and 12-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi et al. (US 6,396,843 B1) in view of Kadambi et al. (US 6,993,027 B1).

3. **Regarding claims 1 and 18,** Chiussi et al. discloses *assigning an exit number to each said packet* (Column 4 lines 45-51, see "schedulers assign increasing values of timestamp [i.e. exit number] to consecutive cells [i.e. packets]..."); *queuing said packets in buffer means* (Column 4 lines 47-51, see "timestamp of the cell at the head of the corresponding cell queue [i.e. buffer means]..."); *allocating said exit numbers to storage bins, each bin accepting a range of orders of exit numbers* (Column 5 lines 18-20, see "one bin associated with each possible value of timestamp...", i.e. exit number; Column 5 lines 32-33, see "each bin is implemented as a list of timestamps...", i.e. range of orders of exit numbers); *and outputting the queued packets in a predetermined order according to an order list determined by said exit numbers assigned to said packets before said packets are queued* (Column 5 lines 20-23, see "bins ordered by increasing value of their corresponding timestamp...", i.e. order list determined by said exit numbers; Column 5 lines 32-38, see "...served in a FIFO...or a LIFO order...", i.e. output of queued packets according to exit number [timestamp]).

Regarding claim 18, Chiussi et al. also discloses the means for performing the aforementioned steps. Specifically, Chiussi et al. discloses *a data manager* (Claim 16, see "...apparatus for services..."), *assigning means* (Column 4 lines 45-51, see "schedulers assign..."), *buffer means* (Column 4 lines 47-51, see "...corresponding cell queue [i.e. buffer means]..."), *storage bins* (Column 5 lines 18-20, see "one bin associated..."), *allocating means* (Column 5 lines 18-20, see "one bin associated with each possible value of timestamp [i.e. exit number]...", allocating means is inherent in this disclosure), *output means* (Column 5 lines 32-38, see "...FIFO...LIFO..."), and *sorting means* (Claim 16, see "...a sorter for sorting the timestamps...").

Chiussi et al. does specifically disclose that *the method is characterized by the step, before said outputting step, sorting the contents of a bin containing a first range of exit numbers into a plurality of bins each containing a smaller range of exit numbers.*

However, Kadambi et al. discloses a method in which a single sorted address table is split into two half-sized tables (i.e. *first range sorted into sets of smaller ranges*) (Column 24 lines 10-15). The splitting allows the two separate tables to remain in sorted order (i.e. *sorting the contents*), and contain entries from the entire address range of the original table (Column 24 lines 19-23). This same logic can be performed on the bins of Chiussi et al. before packets are outputted since each bin is implemented as a list of timestamps [i.e. table of addresses, Kadambi et al.] (Column 5 lines 32-33). The method of Kadambi et al. allows for parallel searching of packet addresses and increased throughput (Column 24 lines 34-37).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the method of dividing a sorted

table of a first range into two separate sorted tables of smaller ranges, in Kadambi et al., into Chiussi et al. in order to allow for parallel (i.e. more efficient) searching of packet addresses and increased throughput.

4. **Regarding claims 3 and 23,** Chiussi et al. in view of Kadambi et al. discloses *placing each said data packet together with its respective exit number in said buffer means, said buffer means comprising said storage bins* (Chiussi et al., Column 4 lines 45-51, see "schedulers assign increasing values of timestamp [i.e. exit number] to consecutive cells [i.e. packets]..."; Column 4 lines 47-51, see "timestamp of the cell at the head of the corresponding cell queue [i.e. buffer means]..."; Column 5 lines15-18, see "calendar queue...ordered structure of bins...", i.e. storage bins).

5. **Regarding claim 9,** Chiussi et al. in view of Kadambi et al. discloses that *bins are FIFO buffers* (Chiussi et al., Column 5 lines 33-35, see "commonly served in a First-In-First-Out (FIFO)...").

6. **Regarding claim 10,** Chiussi et al. in view of Kadambi et al. discloses that *bins are LIFO stacks* (Chiussi et al., Column 5 lines 34-35, see "or a Last-In-First-Out LIFO) order...").

7. **Regarding claim 12,** Chiussi et al. does not specifically disclose that *queue management is performed by (a) processing all of said bins in parallel.*

However, Kadambi et al discloses that searching for two separate packet addresses (i.e. *processing of all bins*) is performed simultaneously, in parallel (Column 24 lines 34-35). This increases throughput (Column 24 lines 34-37).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the parallel processing of Kadambi et al. into Chiussi et al. in order to increase throughput.

Chiussi et al. in view of Kadambi et al. does not disclose that *(b) inserting incoming data into a bin is performed by means of a parallel processor*.

However, it is well known in the art that SIMD processors are used in devices such as Applicant's device (i.e. the apparatus of Chiussi et al. in view of Kadambi et al.) because they are capable of simultaneously performing a single instruction on separate data streams (i.e. *inserting incoming data into a bin*). It is also well known in the art that SIMD processors are parallel processors.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the use of a SIMD processor into the system of Chiussi et al. in view of Kadambi et al. in order to simultaneously perform a single instruction on separate data streams thus increasing throughput in the system.

8. **Regarding claims 13 and 14,** Chiussi et al. in view of Kadambi et al. does not specifically disclose that *the parallel processor is an array processor* and that *the array processor is a SIMD processor*.

However, it is well known in the art that SIMD processors are used in devices such as Applicant's device (i.e. the apparatus of Chiussi et al. in view of Kadambi et al.) because they are capable of simultaneously performing a single instruction on separate data streams. It is also well known in the art that SIMD processors are array processors and parallel processors.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the use of a SIMD processor into the system of Chiussi et al. in view of Kadambi et al. in order to simultaneously perform a single instruction on separate data streams thus increasing throughput in the system.

9. **Regarding claims 15-17 and 19-22,** Chiussi et al. in view of Kadambi et al. does not specifically disclose that *said sorting step is carried out by a parallel processor* (**Claim 15**), *said parallel processor is an array processor* (**Claim 16**), and *said array processor is a SIMD processor* (**Claim 17**) and that *said allocating means comprises a parallel processor* (**Claim 19**), *said sorting means comprises a parallel processor* (**Claim 20**), *said parallel processor is an array processor* (**Claim 21**), and *said parallel processor is a SIMD processor* (**Claim 22**).

However, it is well known in the art that SIMD processors are used in devices such as Applicant's device (i.e. the apparatus of Chiussi et al. in view of Kadambi et al.) because they are capable of simultaneously performing a single instruction on separate data streams. It is also well known in the art that *SIMD* processors are *array processors* and *parallel processors*. Thus, a *SIMD* processor would simultaneously perform the *allocating* and *sorting* steps on separate data streams.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the use of a SIMD processor into the system of Chiussi et al. in view of Kadambi et al. in order to simultaneously perform a single instruction on separate data streams thus increasing throughput in the system.

10. Claims 2 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi et al. in view of Kadambi et al. as applied to claims and 1 and 18 respectively above, and further in view of Turner et al. (US 6,907,041 B1).

11. **Regarding claims 2 and 25,** Chiussi et al. in view of Kadambi et al. does specifically disclose that *said sorting step is repeated until the contents of the bins are completely sorted* and that *said sorting means is adapted to do so*.

However, Turner et al. discloses a merge sorting technique in which sorting is continued in order to produce a single sorted stream of data (i.e. *contents of the bins*), containing the original values in sorted order. This continued sorting is performed until a single sorted stream of data is eventually yielded (Column 2 lines 43-57, i.e. *completely sorted*).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the continued sorting feature of Turner et al. into the system if Chiussi et al. in view of Kadambi et al. in order to produce a single sorted stream of data.

12. Claims 4-6 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi et al. in view of Kadambi et al. as applied to claims 1 and 18 respectively above, and further in view of Chen et al. (US6,829,218 B1).

13. **Regarding claims 4-6 and 24,** Chiussi et al. in view of Kadambi et al. discloses that *said buffer means comprises said series of bins* (**Applicant's claim 24**) (Column 5 lines 18-20, see "one bin associated with each possible value of timestamp...", i.e. exit number; Column 5 lines 32-33, see "each bin is implemented as a list of timestamps...", i.e. range of orders of exit numbers), but does not specifically disclose that *said queuing step comprises placing packet records and said bins are adapted to receive packet records, each record containing information about its respective packet, together with their*

respective exit numbers in said bins (**Applicant's claims 4 and 24**), that *packet records are of fixed length* (**Applicant's claim 5**), and that *packet records are shorter than said packets* (**Applicant's claim 6**).

However, Chen et al. discloses a method and apparatus that implements fair servicing using a fair queuing technique. Chen et al. discloses that the system is particularly suited for systems where the packets/cells are of a fixed size. Chen et al. further discloses that those fixed size packets/cells are stored in bins (Abstract, see All). It is obvious that this teaching will not be beneficial in a system where packets/cells are of a variable size. In order for it to be beneficial in a system where packets/cells are of a variable size, the information stored in the bins has be to something of a fixed size (i.e. *packet records are of fixed length*) and not the packet/cell itself, such as a pointer to the location in memory of the actual packet/cell (i.e. *bin adapted to receive packet records and bin contains packet record containing information about a respective packet*, i.e. *packet records are shorter than said packets* [i.e. pointer to location in memory if obviously shorter than the packet itself]). Thus, by teaching away from the claimed invention in that a bin contains a fixed size **packet/cell**, Chen et al. actually teaches that it is much more beneficial for any information stored in a bin to be of a fixed size, whether the information is the packet/cell itself or information relative to the packet/cell. The method and apparatus of Chen et al. are advantageous in that it is possible to maintain appropriate service of connections without sorting all of the individual connections (Abstract, see "...advantageous in that it is possible...").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the teachings of Chen et al. into

the system of Chiussi et al. in view of Kadambi et al. in order to maintain appropriate service of connections without sorting all of the individual connections.

Allowable Subject Matter

14. Claims 7, 8, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to OTIS L. THOMPSON, JR whose telephone number is (571)270-1953. The examiner can normally be reached on Monday to Thursday 7:30 am to 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag Shah can be reached on (571)272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Otis L Thompson, Jr./
Examiner, Art Unit 2619

April 30, 2008

/Chirag G Shah/

Supervisory Patent Examiner, Art Unit 2619